

WHAT IS CLAIMED IS:

- 1 1. A method comprising:
2 in response to a data read request for requested data:
3 allocating an area of memory to the requested data, the memory
4 area being divided into at least one memory chunk;
5 writing a seed value to one or more of the at least one memory
6 chunk; and
7 in response to completion of at least one write transaction
8 corresponding to the data read request, for each of the one
9 or more memory chunks having a seed value, validating the
10 integrity of each of the at least one write transaction based,
11 at least in part, on the seed value.
- 1 2. The method of claim 1, wherein said validating the integrity of a given one
2 of the at least one write transaction comprises, for a given memory chunk:
3 determining if the memory chunk includes the seed value; and
4 if the memory chunk includes the seed value, determining that the given
5 write transaction is invalid.
- 1 3. The method of claim 2, wherein said determining if the memory chunk
2 includes the seed value comprises determining if the memory chunk
3 includes the seed value at specified bits of the memory chunk.

1 4. The method of claim 2, additionally comprising modifying the seed value if
2 the write transaction is determined to be invalid.

1 5. The method of claim 1, wherein the size of the seed value is based on a
2 specified error rate of the device.

1 6. An apparatus comprising:
2 circuitry capable of responding to a data read request for requested data
3 by:
4 allocating an area of memory to the requested data, the memory
5 area being divided into at least one memory chunk;
6 writing a seed value to one or more of the at least one memory
7 chunk; and
8 responding to completion of at least one write transaction
9 corresponding to the data read request by, for each of the
10 one or more memory chunks having a seed value, validating
11 the integrity of each of the at least one write transaction
12 based, at least in part, on the seed value.

1 7. The apparatus of claim 6, wherein said circuitry capable of validating the
2 integrity of a given one of the at least one write transaction is capable of,
3 for a given memory chunk:
4 determining if the memory chunk includes the seed value; and

5 if the memory chunk includes the seed value, determining that the given
6 write transaction is invalid.

1 8. The apparatus of claim 7, wherein said circuitry capable of determining if
2 the memory chunk includes the seed value is capable of determining if the
3 memory chunk includes the seed value at specified bits of the memory
4 chunk.

1 9. The apparatus of claim 7, wherein said circuitry is additionally capable of
2 modifying the seed value if the write transaction is determined to be
3 invalid.

1 10. The apparatus of claim 6, wherein the size of the seed value is based on a
2 specified error rate of the device.

1 11. A system comprising:

2 a PCI-E (Peripheral Component Interconnect - Enhanced) bus;

3 a buffer communicatively coupled to the PCI-E bus, the buffer being
4 divided into at least one memory chunk; and

5 circuitry capable of responding to a data read request for requested data
6 by:

7 allocating the buffer to the requested data, the buffer being divided
8 into at least one memory chunk;

9 writing a seed value to one or more of the at least one memory

10 chunk; and
11 responding to completion of at least one write transaction
12 corresponding to the data read request by, for each of the
13 one or more memory chunks having a seed value, validating
14 the integrity of each of the at least one write transaction
15 based, at least in part, on the seed value.

1 12. The system of claim 11, wherein said circuitry capable of validating the
2 integrity of a given one of the at least one write transaction is capable of,
3 for a given memory chunk:

4 determining if the memory chunk includes the seed value; and
5 if the memory chunk includes the seed value, determining that the given
6 write transaction is invalid.

1 13. The system of claim 12, wherein said circuitry capable of determining if
2 the memory chunk includes the seed value is capable of determining if the
3 memory chunk includes the seed value at specified bits of the memory
4 chunk.

1 14. The system of claim 12, wherein said circuitry is additionally capable of
2 modifying the seed value if the write transaction is determined to be
3 invalid.

1 15. The system of claim 11, wherein the size of the seed value is based on a
2 specified error rate of the device.

1 16. An article comprising a machine-readable medium having machine-
2 accessible instructions, the instructions when executed by a machine,
3 result in the following:
4 responding to a data read request for requested data by:
5 allocating an area of memory to the requested data, the memory
6 area being divided into at least one memory chunk;
7 writing a seed value to one or more of the at least one memory
8 chunk; and
9 responding to completion of at least one write transaction
10 corresponding to the data read request by, for each of the
11 one or more memory chunks having a seed value, validating
12 the integrity of each of the at least one write transaction
13 based, at least in part, on the seed value.

1 17. The article of claim 16, wherein said instructions that result in validating
2 the integrity of a given one of the at least one write transaction comprise
3 instructions that result in, for a given memory chunk:
4 determining if the memory chunk includes the seed value; and
5 if the memory chunk includes the seed value, determining that the given
6 write transaction is invalid.

1 18. The article of claim 17, wherein the instructions that result in determining if

2 the memory chunk includes the seed value comprise instructions that
3 result in determining if the memory chunk includes the seed value at
4 specified bits of the memory chunk.

1 19. The article of claim 17, additionally comprising instructions that result in
2 modifying the seed value if the write transaction is determined to be
3 invalid.

1 20. The article of claim 16, wherein the size of the seed value is based on a
2 specified error rate of the device.